REMARKS

The Examiner's Office Action of February 19, 2004 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

Claims 1 and 75-96 are pending for consideration, as claims 2-74 have been previously cancelled. Claims 1 and 75-80 are independent. In view of the following remarks, reconsideration of this application is now requested.

Referring now to the detailed Office Action, claims 1 and 75-96 stand rejected under the judicially created doctrine of obviousness-type double patenting as unpatentable over claims 1-12 of U.S. Patent No. 6,472,684 in view of Akbar, Yamazaki et al. and Koyama (U.S. Patent No. 5,793,344), and claims 1 and 75-96 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-30 of U.S. Patent No. 6,509,602 in view of Akbar, Yamazaki et al. and Koyama. In response, Applicants respectfully request that these double patenting rejections be held in abeyance until all pending claims are found allowable.

Claims 75, 76, 85, 86, 91 and 92 stand rejected under 35 U.S.C. §102(b) as anticipated by Koyama (U.S. Patent No. 5,793,344). Further, claim 1 stands rejected under 35 U.S.C. §103(a) as unpatentable over Yamazaki et al. (JP 11-154714 and the Derwent Translation of this document) and Akbar (U.S. Patent No 5,656,845). These rejections are respectfully traversed at least for the reasons provided below.

With respect to the rejection of claims 75, 76, 85, 86, 91 and 92 under 35 U.S.C. 102(b) as anticipated by Koyama, the Examiner contends that Koyama discloses:

a substrate 110 and a non-volatile memory 115 over the substrate;

a pixel portion 111 over the substrate;

a source wiring driver circuit 113 over the substrate;

a gate wiring driver circuit 112 over the substrate;

a correction circuit 116 over the substrate;

a memory controller circuit 114 over the substrate.

However, Applicants respectfully assert that Koyama does not teach that the above circuits are over the same substrate as recited in claims 75 and 76. More specifically, Koyama does not disclose a substrate, non-volatile memory over the substrate, a pixel portion

over the substrate, a source wiring driver circuit for driving the pixel portion over the substrate, a gate wiring driver circuit for driving the pixel portion over the substrate, and a correction circuit over the substrate as recited in pending claim 75. Further, Koyama does not disclose a substrate, a non-volatile memory over the substrate, a pixel portion, a source wiring driver circuit for driving the pixel portion over the substrate, a gate wiring driver circuit for driving the pixel portion over the substrate, and a memory controller circuit over the substrate for controlling the non-volatile memory circuit as recited in pending claim 76.

Moreover, Applicants respectfully assert that Fig. 1 of Koyama relied on by the Examiner cannot be used to determine that the claimed circuits are over the same substrate, as alleged by the Examiner, because Fig. 1 showing a high level diagram does not disclose any specific support for the Examiner's assertion.

Still further, Applicants respectfully submit that the Examiner is erroneous in contending that 110 is a substrate when in fact element 110 is a LCD device (see col. 4, line 15 of Koyama). Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Koyama, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 75, 76, 85, 86, 91 and 92, under 35 U.S.C. §102(b), as anticipated by Koyama, is improper.

With respect to the rejection of claim 1 under 35 U.S.C. §103(a), claim 1 as unpatentable over Yamazaki et al. (JP 11-154714 and the Derwent Translation of this document) and Akbar, the Examiner acknowledges that Yamazaki et al. does not disclose the first and second semiconductor layer in a common semiconductor island. To cure the deficiency of Yamazaki et al., the Examiner applies Akbar as disclosing a first and second semiconductor layer in a common semiconductor island with improved performance and reliability. However, Applicants respectfully assert that neither Yamazaki et al. nor Akbar provide any motivation or suggestion to combine their respective teachings to arrive at Applicants' invention as recited in claim 1.

On page 4, second paragraph of the Office Action, the Examiner cited col. 2, lines 19-22 of Akbar as disclosing the motivation to combine Akbar's EEPROM's first and second layer on a common semiconductor island to improve performance and reliability. However, Applicants respectfully assert that the Examiner has cited col. 2, lines 19-22 completely out of context. As disclosed by Akbar, the object of Akbar's invention is to overcome the

problem of imperfection in a silicon layer immediately beneath a tunnel dielectric window of a floating gate transistor and to improve performance and reliability of a non-volatile semiconductor memory cell. Applicants respectfully assert that Akbar does not teach, disclose or suggest combining or modifying its first and second layer on a common semiconductor island with the teachings of Yamazaki et al. to arrive at Applicants' claim 1.

Moreover, as submitted in the Amendment of November 21, 2003, Akbar does not teach or suggest that the floating gate electrode comprises one of tantalum and tantalum alloy and the second insulating film comprises an oxide thereof.

It is well settled that when combining the references in order to support a *prima facie* case of obviousness, the references must be considered in their entirety. It is further settled that the mere fact that the prior art may be modified to reflect features of the claimed invention does not make the modification and hence the claimed invention obvious unless the desirability of such modification is suggested by the prior art itself. Moreover, the claimed invention cannot be used as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious, In Re Fritsch, 23 USPQ2d 1780 (Fed. Cir. 1992). As the Examiner fails to provide motivation or suggestion to modify the respective teachings of Yamazaki et al. and Akbar to make Applicants' invention as recited in claim 1, as discussed above, the §103(a) rejection of claim 1 is insupportable.

With respect to the §103(a) rejection of claims 77-84, 87-90 and 93-96 over Yamazaki et al. and Akbar, as applied to claims 75, 76, 85, 86, 91 and 92 above, and further in view of Koyama, Applicants respectfully submit that the arguments set forth above in relation to the §102(b) rejection of claims 75, 76, 85, 86, 91 and 92 and the §103(a) rejection of claim 1 are also applicable. More specifically, as Koyama fails to disclose Applicants' claimed substrate and circuits over the same substrate, and as Akbar fails to suggest or motivate combining its first and second semiconductor layers in a common semiconductor island with Yamazaki et al., the combination of Yamazaki et al., Akbar and Koyama is insupportable.

In view of the arguments set forth above, Applicants respectfully request reconsideration and withdrawal of all the pending rejections.

While the present application is now believed to be in condition for allowance, should the Examiner find some issue to remain unresolved, or should any new issues arise, which

could be eliminated through discussions with Applicants' representative, then the Examiner is invited to contact the undersigned by telephone in order that the further prosecution of this application can thereby by expedited.

Respectfully submitted,

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